

# Introduction of TFT R&D Activities in Seiko Epson Corporation

Tatsuya Shimoda

Technology Platform Research Center, Seiko Epson Corporation  
281 Fujimi, Fujimi-machi, Suwa-gun, Nagano-ken 399-0293 Japan

## Abstract

Introduced are research activities that are under way at Seiko Epson Corporation under the company's "TFT New Age" program. The program includes R&D projects geared toward achieving high-performance TFTs, developing flexible electronic devices through the use of SUFTLA-TFT technology, and adopting a micro-liquid process for fabricating displays.

## 1. Introduction

Amorphous-Si TFTs are fabricated in fairly high numbers and have become established as an essential device for the display industry. Poly-Si TFTs, meanwhile, have been playing a minor role in the electronics industry, apart from their use in a light-valve application for LCD projectors. The reason that poly-Si TFTs have been relegated to a minor role is because they are considered a half-finished device compared to amorphous-Si TFTs and bulk MOSFETs. In other words, crystallized TFT technology has not been exploited to the extent where it is used in large applications.

Around 10 years ago we at Seiko Epson Corporation (SEC) launched a new R&D program that we named "TFT New Age." The objective of the program is to find attractive new applications for TFTs by both pushing the Si-TFT performance envelope and by creating added value[1-3]. The program consists of three major projects: (1) a project to develop high-performance TFTs that includes understanding and enhancing transistor physical properties while reducing transistor size; (2) a project to develop flexible microelectronics devices by exploring SUFTLA-TFT technology; and (3) a project to adopt a micro-liquid process. These projects have been strongly supported by efforts to find new TFT applications and to explore TFT circuit design tools. While poly-Si TFTs have been the main target for these projects, organic TFTs are one of the themes being explored in conjunction with the micro-liquid process program.

## 2. High-performance TFTs

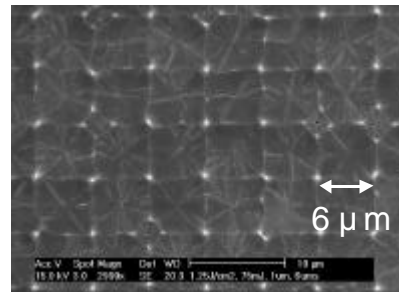
We have been conducting R&D in both low-temperature polysilicon TFTs (LTPS) and high-temperature polysilicon TFT (HTPS) fields. This paper focuses only on research in the LTPS field. Although LTPS properties have been continuously improving, a wide gap still exists between LTPS and MOSFETs in terms of properties and reliability. An obstacle to the development of a high-performance Si-TFT having properties comparable to those of MOS-SOI is the existence of grain boundaries. Even if defects in grain boundaries and inside of a grain were carefully eliminated, this obstacle would remain. Therefore, our ultimate objective with respect to high-performance TFTs is to obtain a TFT in which the channel comprises a single-grain Si. (Of course, once such a TFT is achieved, it will no longer deserve to be called LTPS!) A second objective here is to reduce the TFT size without sacrificing the inherent advantages of TFTs, a requirement if TFTs are to compete with MOS-SOI.

### 2-1 Single grain Si-TFT

#### (1) Formation of a single-grain array

Delft University and Seiko Epson have jointly developed a unique crystallization method called the micro-Czochralski (grain-filter) process that enables us to place a location-controlled Si single grain in the desired position of a substrate. The typical fabrication process of the single-grain Si-TFT is as follows.

Thermally oxidized crystal-Si wafers are patterned by plasma etching into a grid featuring 0.75- $\mu\text{m}$ -deep cavities having a diameter of 1.0  $\mu\text{m}$ . Subsequently, a silicon dioxide is deposited by PECVD using TEOS and oxygen at 350  $^{\circ}\text{C}$ . The diameter of the cavities is automatically decreased down to less than 100 nm. Next, a 250-nm-thick a-Si is deposited by LPCVD using silane at 545  $^{\circ}\text{C}$ . Upon XeCl excimer-laser ( $\lambda = 308$  nm, pulse duration=56 ns) irradiation with optimized energy, a small unmolten Si region remains at the bottom of the cavities. As cavity diameter is sufficiently small compared with the depth, only one solid-seed would remain in such a Si column during crystal growth from the bottom seed. Even if more than one seed were to remain in the Si



**Figure 1.** An array of single grains formed by the micro-Czochralski (grain-filter) process.

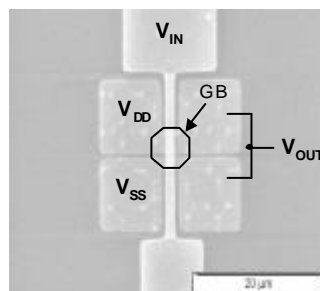
column, only one is "filtered out" after vertical growth along the thin column. Immediately after the surviving single crystal reaches the top of the Si-column, it becomes the seed for vertical crystallization that spreads radially until the crystal collides with the crystal growing

from the adjacent grain-filter. This enables us to obtain an array of single, rectangular grains, as shown in Figure 1.

#### (2) CMOS inverter circuits

The n-channel Si-TFTs fabricated inside a location-controlled grain by the micro-Czochralski process showed a field-effect electron mobility  $\mu_{FEe}$ , subthreshold slope  $S$  and off-current of 597  $\text{cm}^2/\text{Vs}$ , 0.20 V/dec and  $\sim 10^{-13}$  A, respectively [4]. Meanwhile, their p-channel counterpart showed a  $\mu_{FEp}$ ,  $S$  and off-current of 250  $\text{cm}^2/\text{Vs}$ , 0.29 V/dec. and  $\sim 10^{-13}$  A, respectively [5]. Now, we are ready to fabricate CMOS circuits.

Last year we announced the development of a CMOS inverter circuit composed of two single-crystal TFTs inside a location-controlled grain, i.e. a single-grain CMOS inverter [6]. The same process as that described above was used to fabricate the



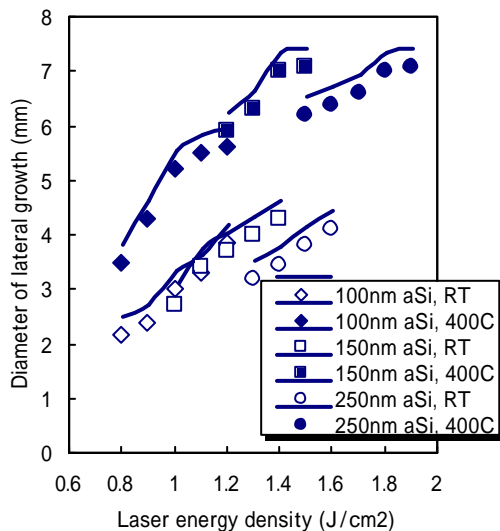
**Figure 2.** The single-grain CMOS inverter.

single-grain grid having a spacing of 5  $\mu\text{m}$ . After the single grains were formed, oxygen plasma treatment was carried out. The crystallized Si film was then patterned into islands. The channel region of both the n-channel TFT and p-channel TFT is designed so that a single grain covers the entire channel area of both TFTs, as shown in Figure 2. After an 89-nm layer of

SiO<sub>2</sub> was deposited by ECR-PECVD to serve as a gate insulator, Al was sputtered and patterned as the gate electrode. The source and drain regions were implanted with phosphorous and boron to form n- and p-channel Si-TFTs. This was followed by excimer-laser activation. To determine the propagation delay of one stage, ring oscillators were also fabricated by a chain of single-grain CMOS TFT inverters. Measured channel widths were 2.75 μm for p-channel TFTs and 1.43 μm for n-channel TFTs, whereas channel length was 1.24 μm for both types of TFT. The field effect mobilities of n- and p-channel Si-TFTs were 425 cm<sup>2</sup>/Vs and 205 cm<sup>2</sup>/Vs, while the subthreshold voltage of n- and p-channel Si-TFTs were estimated to be -3.0 V and +0.5 V, respectively. The obtained inverters showed a full rail-to-rail swing and full-range abrupt voltage transfer characteristics. The 31-stage ring oscillator that was fabricated oscillated with a frequency of 53.4 MHz with a power supply voltage V<sub>DD</sub> of 10V. The propagation delay is estimated to be 0.6 ns/stage.

### (3) Single grain Si-TFTs on a glass substrate

There is a pressing need to fabricate single-grain Si-TFTs on a large glass substrate if we are to exploit the inherent advantages of TFTs. But adopting the micro-Czochralski process had not been a straightforward task due to difficulties in forming a good grain filter. As will be discussed below, conventional exposure systems for glass substrates have low resolution. The low resolution precludes cavities having a diameter of less than 1 μm. Fortunately, however, we now can avail ourselves of a novel exposure system called a Holographic Mask Aligner (HMA) that can guarantee dimensions as precise as 0.5 μm. The experimental procedure used to form a single-grain Si-TFT on a glass substrate is as follows [7]. First, small holes with a diameter of 0.6 μm and a depth of 650 nm are formed in SiO<sub>2</sub> film deposited on a 300 x 300 mm<sup>2</sup> glass substrate by using the HMA and inductive coupled plasma (ICP) etching systems. Second, a 550-nm-thick TEOS PECVD SiO<sub>2</sub> film was deposited over the structure to reduce the diameter of the cavity to around 100 nm. Then, an a-Si film with a thickness of 150 nm was deposited and crystallized by laser irradiation so as to



**Figure 3.** Diameters of Si lateral growth as a function of laser energy density for various a-Si thickness and substrate temperatures.

form an array of single grains. Figure 3 shows grain growth dependence on the laser power. A maximum diameter of around 7 μm was obtained. This number is larger than that obtained on a Si wafer [8]. A gate insulator with a thickness of 40 nm was prepared by TEOS-PECVD and annealed at 330°C for an hour in a steam ambient. Single-grain TFTs were fabricated at a shifted position from the grain-filter. A Si-TFT with a 1-μm channel length and a 1.7-μm channel width had a field-effect mobility of 512 cm<sup>2</sup>/Vs and a subthreshold swing of 0.16 V/dec, on average, at a drain voltage of 0.1V.

## 2-2 Size reduction of TFT

### (1) Holographic Mask Aligner

One of the advantages of TFTs is that they can be fabricated on large, inexpensive substrates made of glass, plastic, stainless steel, and so forth. But these substrates have inherent surface undulations of around 10 μm. To accommodate such large undulations and print patterns on glass substrates, an exposure system has to have a large depth of focus (DOF). On conventional exposure systems, DOF is obtained at the expense of resolution. Resolution has conventionally been constrained to 1.5 μm on large glass substrates, with further advances being very difficult to achieve.

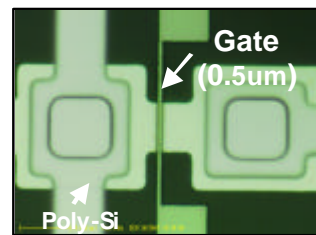
A novel microlithography system that achieves 0.5-μm photoresist patterning on a large glass substrate using total internal reflection (TIR) holography [9] has been developed through technical collaboration between Holtronic Technologies, GSI Creos Corporation and SEC. The developed machine, named the HMA-500SF, works on TIR holography principles [10]. First, a holographic mask is generated from the original patterning information on a chromium (Cr) mask by holographic recording, wherein an object beam that passes through the Cr mask interferes with a reference beam that scans synchronously with the object beam. The second step is called "hologram replay": a scanning replay beam passes through the holographic mask, reconstructing the original pattern of the Cr mask onto the layer of photoresist coated on the glass substrate. The HMA-500SF is also equipped with a dynamic focusing system. As the replay beam is scanned, the system sequentially measures the gap between the holographic mask and the glass substrate and controls the height of the substrate chuck so as to keep the gap constant. Hence, the HMA-500SF achieves 0.5-μm line patterning on 300 x 300 mm<sup>2</sup> glass substrates, even on those having poor surface uniformity.

### (2) Fine etching

An ICP etcher is used for fine pattern etching. A high-density plasma source is made by inductive coupling produced by applying RF power for the spiral coil and bias power to the substrate. Using this system, we succeeded in etching 0.5-μm lines of gate electrodes on 300 x 300 mm<sup>2</sup> glass substrates with a high etching rate and low etching damage [11].

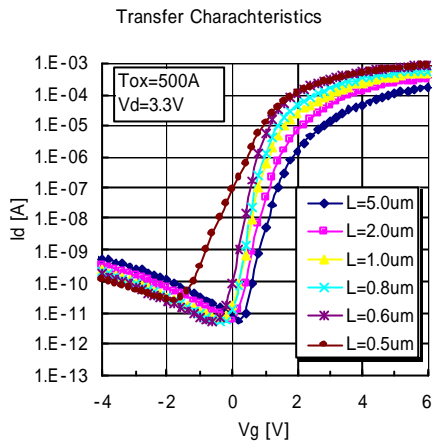
### (3) Fine-gate TFT [11]

We fabricated fine-gate poly-Si TFTs having a channel length L of only 0.5 μm on a 300 x 300 mm<sup>2</sup> glass substrate. A 50-nm-thick a-Si on a SiO<sub>2</sub> buffer layer was crystallized by XeCl laser, converting it into a poly-Si film having grains approximately 0.3 μm in diameter. After the poly-Si was patterned, a gate film (TEOS-SiO<sub>2</sub>) was deposited to a thickness of 50 nm. Tantalum (Ta) narrow gates



**Figure 4.** Photograph of the TFT with the 0.5-μm gate length.

having a length of from 5  $\mu\text{m}$  to 0.5  $\mu\text{m}$  were precisely formed by using the HMA-500SF and ICP etcher.



**Figure 5.** The transfer characteristics of n-channel TFTs fabricated with varying lengths but the same 10- $\mu\text{m}$  gate width  $W$ . The graphs in Figure 5 show the

transfer characteristics of n-channel TFTs fabricated with varying lengths but the same 10- $\mu\text{m}$  gate width  $W$ . TFT characteristics shift to the reverse side of the gate bias as  $L$  is reduced, but we confirmed the switching characteristics of TFTs with an  $L$  of 0.5  $\mu\text{m}$ .

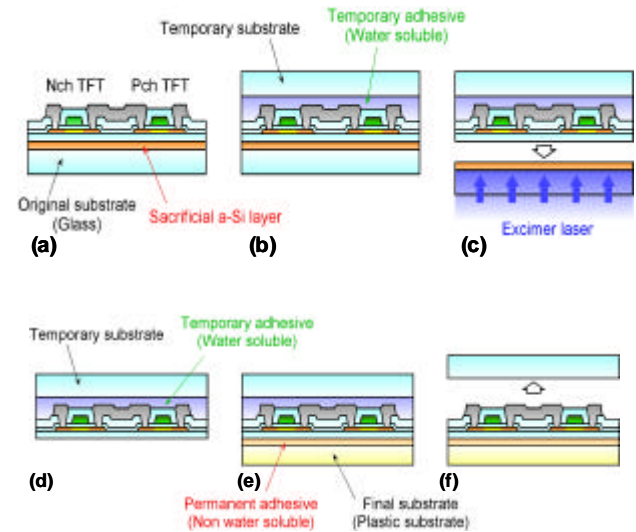
### 3. Flexible microelectronics devices

SUFTLA (Surface Free Technology by Laser Ablation) is a transfer technology that realizes TFT circuits on a flexible substrate [12]. This technology has been used to develop several flexible devices. In the display field, we developed a high-resolution, 0.4-inch active-matrix LCD; a 2-inch colour active-matrix organic light-emitting diode (AM-OLED) display; and a small-sized, active-matrix electrophoretic display (AM-EPD). In addition to displays, we developed a TFT fingerprint sensor having 304 scan lines and 304 data lines with a resolution of 385 dpi. The sensor operates at low voltage, less than 3V. We also recently developed an 8-bit microprocessor containing 32,000 transistors on a plastic substrate.

#### 3-1 SUFTLA<sup>®</sup> Technology

The Si-TFT transfer process is usually completed after two transfer steps. The Si-TFT layer is once transferred from an original substrate to a temporary substrate, and it is transferred again from the temporary substrate to a final substrate. Figure 6 shows schematic illustrations of the SUFTLA process. In the beginning, a 100-nm-thick a-Si thin film is deposited by chemical deposition (CVD) on the original glass substrate, as shown in (a). This a-Si works as a sacrificial layer, releasing the Si-TFT circuit during the first transfer step. A CMOS poly-Si TFT device is then fabricated on the a-Si sacrificial layer by using a conventional LTPS process. The crucial point in this technology is that absolutely no special techniques or special apparatuses are needed in the LTPS TFT fabrication step. Next, the surface of the Si-TFT devices is glued on a temporary glass substrate using a water-soluble temporary adhesive that is cured by UV light, as shown in (c). The a-Si sacrificial layer is then irradiated by a 308-nm XeCl excimer laser from the backside of the original substrate. Excimer laser irradiation abruptly heats the a-Si layer and causes it to melt and re-crystallize with fairly large roughness;

irradiation also causes hydrogen atoms contained in the CVD a-Si



**Figure 6.** The process flow of SUFTLA (Surface Free Technology by Laser Ablation) that is a transfer technology that realizes TFT circuits on a flexible substrate.

layer to be released at the interface between the sacrificial layer and Si-TFT layer. Both of these phenomena reduce the adhesion force at the interface, resulting in easy separation of the Si-TFT device from the original substrate, as shown in (d). The Si-TFT device is not damaged during the laser irradiation process because the laser power is completely absorbed into the a-Si layer. The same Si-TFT properties are observed before and after the laser irradiation process [12]. After the Si-TFT device is transferred onto the temporary substrate, the backside of the Si-TFT device is glued on the final substrate using a permanent adhesive, as shown in (e). A flexible plastic film is usually used as the final substrate. Soaking the sample in water dissolves the temporary adhesive so as to remove the temporary substrate from the Si-TFT device, as shown in (f). The first Si-TFT device that we fabricated was a 15-stage CMOS ring oscillator using LTPS. Perfect operation was confirmed: the frequency is 405.68 kHz at  $V_{dd}=10\text{V}$  and 1.83 MHz at  $V_{dd}=15\text{V}$  [12].

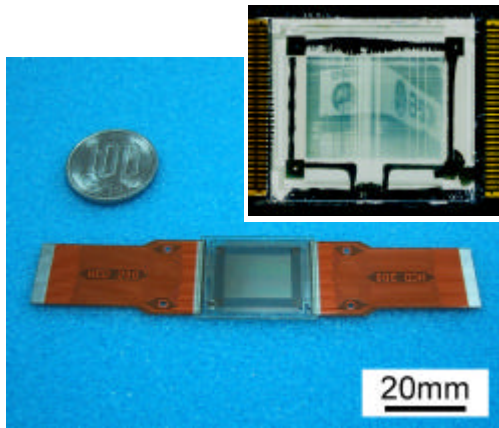
#### 3-2 Flexible Displays

We have been developing a series of flexible active-matrix displays by combining a SUFTLA TFT backplane with different kinds of display media: an AM-LCD in 2001 [13], a monochrome AM-OLED in 2002 [14], a colour AM-OLED in 2003 [15], and an AM-EPD in 2004 [16]. With the SUFTLA TFT backplane, not only pixel TFTs but also peripheral TFT drivers are fabricated on a plastic substrate.

##### (1) Flexible AM-LCD

The flexible AM-LCD that we fabricated is a small, monochrome panel measuring 0.7-in. in diagonal. It has  $428 \times 238$  pixels. The pixel pitch, or pixel area, is  $34 \mu\text{m} \times 46 \mu\text{m}$ . Frame frequency is 60 Hz. For the data driver, a series of four 107-stage static shift registers is integrated and is driven by an analog point-time scheme at the frequency of 1.4 MHz using the driving voltage of 12V. For the scanning driver, a series of two 119 stages static shift registers plus 238 NAND gates are integrated. Its clock frequency is 4 kHz. The entire Si-TFT circuit, including the pixel array and the peripheral drivers, were transferred onto a 400- $\mu\text{m}$ -thick transparent plastic substrate. This plastic substrate was used to

assemble an LCD module using a standard LCD process. A 400- $\mu\text{m}$ -thick transparent plastic substrate with sputter-deposited ITO electrode was used as the counter substrate. During the LCD assembly process, the process temperature was kept below 120 °C, because the Si-TFT backplane exhibits weak heat resistance due to the difference of the thermal expansion coefficient between the plastic substrate and the Si-TFT layer. We certified the proper operation of the data and the scan drivers by observing the output waveform of both drivers. Figure 7 shows the outward appearance



**Figure 7.** The flexible AM-LCD module and its display image and the display image [13].

## (2) Flexible AM-OLED

The TFT circuit we used was already reported in detail elsewhere [17]. We modified it for the SUFTLA process and tried to transfer the Si-TFT circuit to a plastic substrate. The specifications of the Si-TFT circuit are summarized in Table 1. The OLED measures 5.3  $\times$  5.1 cm<sup>2</sup>. The pixel circuit was designed to drive in area ratio grayscale (ARG) mode. Each pixel consisted of plural

Display specifications	
Diagonal	5.3cm (2.1inch)
Pixel number	200 x 150
Pixel pitch	211.5mm (120ppi)
Sub-pixel pitch	70.5mm
Driving scheme	ARG+TRG, line-at-a-time
Typical driving conditions	
Clock frequency	Signal driver 333kHz
	Scanning driver 5.0kHz
Driving voltage	Signal driver 6.0-8.0V
	Scanning driver 6.0-8.0V
	LEP 3.0V

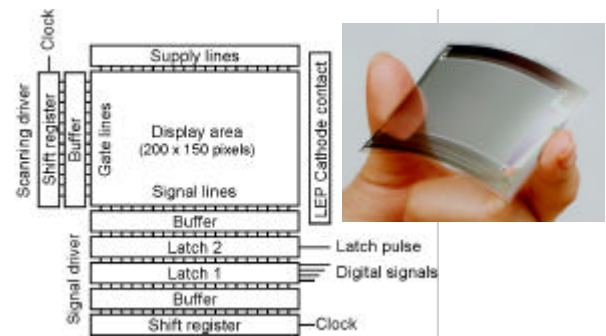
**Table 1.** The specification of the flexible OLED displays.

integrated driver circuits drive the display area in digital line-at-a-time mode. A scanning driver includes a static-type shift register having 150 stages, which is designed to operate at a clock frequency of 5 kHz. The signal driver consists of a series of plural circuits connected in parallel. They are placed in the order of a buffer, latch 1, latch 2, a buffer and a shift register circuit having 50 stages from the pixel area. The shift register is designed to operate at a clock frequency of 333 kHz. The output pulse of the shift register is applied to latch 1 through the buffer circuit, and the digital signals input in

of plural sub-pixels, which are controlled to be in either the completely on state or completely off state. Since there are nine sub-pixels in each pixel, ten grayscales can be achieved in the case of a monochrome display. The

24 parallel state are stored in latch 1. After sampling all the digital signals for the selected gate line, a latch pulse is input and the digital signals are transferred into the display area through latch 2.

Figure 8 shows the appearance of the TFT-OLED backplane after being transferred onto the plastic substrate and the block diagram of circuits. After the transfer process, correct driver circuit operation was confirmed. The TFT-OLED backplane was subsequently forwarded to the OLED assembly process. For a colour OLED display, the OLED materials are patterned using an inkjet printing technique. The OLED panel was 0.7-mm thick and weighed 3.2g, making it both far thinner and lighter than an ordinary glass-based TFT-OLED panel.



**Figure 8.** The appearance of the TFT-OLED backplane after being transferred onto the plastic substrate and the block diagram of OLED circuits.

## (3) Flexible AM-EPD

The active-matrix electrophoretic display (AM-EPD) that we developed has a display area of 8.4 mm  $\times$  61.5 mm, and 24  $\times$  176 pixels. The resolution is 73 dpi, which corresponds to a pixel pitch



**Figure 9** The photograph of AM-EPD devices formed on both a glass substrate and on a flexible one.

of 350  $\mu\text{m}$ . A large storage capacitor is formed in each pixel so that the driving electric field can be kept sufficiently strong during a writing period. As EPD writing generally takes a relatively long time, we used

line-at-a-time mode in order to avoid crosstalk. A two-phase driving scheme comprising a reset-phase that erases a previous image and a writing-phase for writing a new image was chosen to cope with the EPD's high driving voltage. The introduction of this scheme enables the AM-EPD to operate successfully with a driving voltage of 8.5V. That enabled us both to reduce the voltage for EPD and to avoid Si-TFT degradation at high operating voltage. Figure 9 shows a photograph of AM-EPD devices formed on both a glass substrate and on a flexible one. The flexible TFT backplane was formed using the SUFTLA process. The first step in the AM-EPD fabrication sequence was to prepare an electrophoretic (EP) sheet by coating a PET film bearing an ITO layer with electrophoretic materials. The EP sheet thus obtained

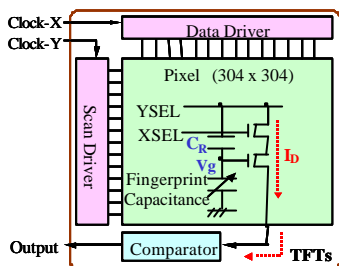


was 155  $\mu\text{m}$  thick. The EP sheets were then laminated onto a glass or a flexible TFT backplane. The total thickness of the glass AM-EPD was 855  $\mu\text{m}$ , while that of the flexible AM-EPD was 375  $\mu\text{m}$ .

### 3-3 Flexible microelectronics devices

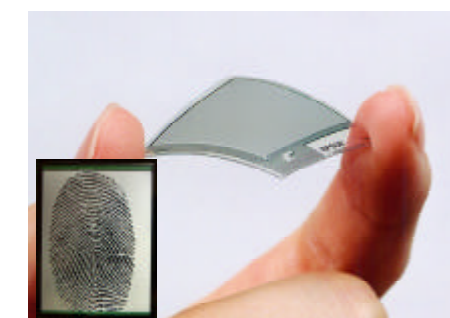
#### (1) Flexible TFT fingerprint sensor

We developed a TFT fingerprint sensor (TFT-FPS) [18]. Our sensor reads the surface contours of a fingerprint by detecting electrostatic capacitance,



**Figure 10.** The block diagram of the Si-TFT circuit of the TFT-FPS.

which changes according to the depth of the fingerprint valleys. The TFT-FPS consists of active-matrix pixels, a data driver, a scan driver and a comparator. It has 304 scan lines and 304 data lines in a matrix of 304 rows and 304 columns. The TFT-FPS operates in a manner quite similar to that of an AM-LCD. Figure 10



**Figure 11.** The flexible TFT-FPS and its fingerprint image taken at  $V_{\text{dd}}=4\text{V}$ .

shows a block diagram of the Si-TFT circuit of the sensor. The pixel includes a capacitance-detecting electrode, a capacitance-detecting dielectric layer, a reference capacitor ( $C_r$ ) and a signal-amplifying element. Operation details are described elsewhere [18]. The Si-TFT sensor is larger than a standard bulk Si fingerprint sensor thanks to a glass substrate. The 304-dpi resolution is sufficient for personal identification. The frame frequency is 5.41 Hz. The operating voltage of the TFT sensor, 2.5V – 5.0V, ranges nearly the same as that of the standard bulk Si sensor. SUFTLA technology enables the Si-TFT fingerprint sensor to be easily and completely transferred to a plastic substrate with neither severe degradation of Si-TFT properties nor fatal mechanical damage. Figure 11 shows the flexible TFT-FPS and its fingerprint image taken at  $V_{\text{dd}}=4\text{V}$ .

#### (2) Flexible 8-bit asynchronous microprocessor

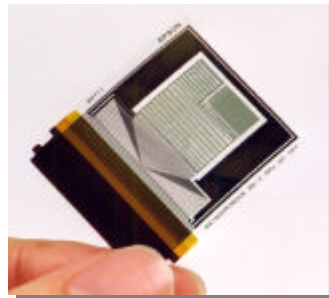
A flexible 8-bit asynchronous microprocessor, ACT11, based on LTPS technology, SUFTLA technology and the Verilog+ asynchronous circuit design language was developed. Table 2 lists the specification. One of drawbacks of LTPS is that they have substantial deviations in characteristics, primarily due to deviations in crystal grain size and silicon-oxide thickness. Until recently, these deviations were considered to be beyond the capability of synchronous circuit design, especially for large-scale circuits driven by global clocking. Since asynchronous circuits are “self-timed,” they absorb the deviations of device characteristics.

Technology	Poly-Si TFT CMOS, 2 Metal Layers TFT L/W( $\mu\text{m}$ ) : 4/12(Nch) & 4/36(Pch)
Elements	~32,000 Transistors
CPU Architecture	608 Instructions incl MLT & DIV 16MByte Addressing Space BUS Release for BUS Masters Outside 4 Interrupt Sources Synchronous BUS Interface
Supply Voltage	3~6V
Clock	500KHz Max.
Dimensions	27.0mm x 24.0mm x 0.2mm (Core: 12.5mm x 12.5mm x 0.2mm)
Weight	140mg (+100mg FPC)
I/O Pins	80 Pins

**Table 2.** The specification of the flexible CPU.

In addition, they run as fast as possible in event-driven fashion while dissipating less power and remain in standby for quick service.

Using SUFTLA, the approximately 4 $\mu\text{m}$ -thick TFT layer of ACT11, an asynchronous CPU fabricated of LTPS, is lifted off the glass substrate for transfer to a plastic substrate, as shown in Figure 12 [19].



**Figure 12.** The flexible 80bit CPU.

Even with the benefits of asynchronous circuits, it is still difficult to design circuits using syntax-directed translation with VLSI programming languages. Verilog+ was developed to address this. Verilog+ comprises a subset of Verilog HDL<sup>®</sup> and minimal primitives used for describing the communications between processes. ACT11 is the first successful instance of asynchronous design using Verilog+.

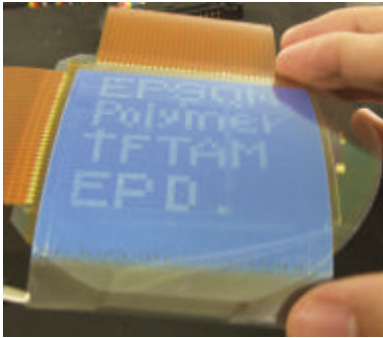
The design of ACT11 can be verified with the set of 608 instructions that is compatible with the synchronous counterpart. The result shows that ACT11 consumes about 70% less power than the synchronous design, with 21 dB less electromagnetic emission. The ACT11 chip operates from 3.5V through 7V. One of the most serious problems found in a high-performance processor on plastics is that low thermal conductivity of plastic materials causes overheating, which precludes full operation of a processor on plastics. Full operation was made possible without any loss of processor performance as the power dissipation decreased markedly compared to the synchronous counterpart.

#### 4. The adoption of a micro-liquid process

A micro-liquid process (MLP) is a new kind of additive process in which a liquid material is directly applied only where needed on a substrate. Compared to the conventional process, which consists mainly of vapor deposition and photolithography, the new method promises greater efficiency in the use of materials, simpler manufacturing processes, and a smaller apparatus footprint. An inkjet printing system is one of the tools in this process. The system ejects droplets and places them in desired locations on a substrate at accuracy of around 10  $\mu\text{m}$ . For more precise patterning, we can use the ability of droplets to self-assemble when they land on a substrate pre-patterned with hydrophobic and

hydrophilic regions. By carefully controlling solvent drying, we can obtain a patterned solid thin film with uniform thickness.

Light-emitting polymers, organic semiconductors, and other organic materials are quite compatible with liquid processes. We used these organic materials to develop a colour filter for use in LCD, organic electroluminescent diodes for OLED displays [20,21], organic TFTs and TFT circuits [22,23]. We recently announced the development of a 32 x 32 pixel EPD operated by an organic TFT active-matrix backplane both on a glass substrate [24] and a plastic substrate [25]. Figure 13 shows a display image of



**Figure 13.** The flexible EPD driven by the organic TFT backplane.

the EPD operated by the organic TFT backplane fabricated mainly by MLP.

Several kinds of liquid metal material such as Ag, Au, Cu, Pt, Pd, were already developed in the worldwide. We used a Ag liquid material, which composed of Ag nano-particles suspended an organic solvent [26], to inkjet-print bus lines for a plasma display

panel (PDP) and gate electrodes for organic TFTs [24].

One of the objectives of the micro-liquid process is to fabricate poly-Si TFTs. For this purpose we need to develop or synthesize several liquid materials: Si, SiO<sub>2</sub>, metals, n-dopant and p-dopant. Among them we successfully applied liquid SiO<sub>2</sub> material to Si-TFT and obtained a TFT having a field-effect mobility of 33.2 cm<sup>2</sup>/Vs [27]. Liquid Ag and Cu materials have already been developed and are ready to be adopted for Si-TFT. As for the other materials, we are very optimistic about developing or finding them, thus enabling us to soon fabricate Si-TFTs.

#### 4. Summary

I introduced three major projects carried out in SEC under the name of TFT New Age program; high-performance Si-TFTs, flexible microelectronics devices and adoption of a micro-liquid process to TFTs. In the program of high-performance Si-TFTs, we developed a unique crystallization method called the micro-Czochralski (grain-filter) process which enable us to have single-grain TFTs having a mobility compatible with that of a bulk MOSFET. CMOS inverter circuits and a 31-stage ring oscillator constructed were developed using the single-grain TFTs. The propagation delay of the oscillator was so small as estimated to be 0.6 ns/stage. For reduction of the TFT size, a novel micro-lithography system that achieves 0.5- $\mu$ m photoresist patterning on a large glass substrate was developed using total internal reflection (TIR) holography. We confirmed the switching characteristics of poly-Si TFTs with an L of 0.5  $\mu$ m. In the program of flexible microelectronics devices, not only flexible displays including an AM-LCD, AM-OLEDs and an AM-EPD, but also a fingerprint sensor and even an asynchronous CPU were developed by using SUFTLA process. Finally, in the program of adoption of a micro-liquid process to TFTs, organic TFTs and an AM-EPD driven by organic TFTs backplane were developed. As a main fabrication technology an inkjet printing was used. Liquid metals and liquid SiO<sub>2</sub> materials were successfully adopted to TFTs. I believe it is not so long before adoption of a micro-liquid process to fabrication of Si-TFTs becomes realistic.

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