Single-Grain Si TFTs Fabricated by the mCzochralski (Grain-Filter) Process on a Large Glass Substrate

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Location-controlled Si grains are prepared on a large glass substrate for the first time by the μ-Czochralski (grain-filter) process. The maximum diameter of the Si grains is around 7 μm, and EBSD and TEM analysis show that the Si grains contain few defects except coincidence site lattice (CSL) boundaries. Owing to the crystalline quality of the Si grains, single-grain Si TFTs obtained from the process give a high field-effect mobility of 512 cm^2/Vs and a low subthreshold swing of 0.16 V/dec.

1. Introduction

Single-grain Si (sg-Si) TFTs fabricated on glass have been a key technology for not only future System on Glass, but also System on Plastic, which can be realized with SUFTLA technology[1)]. For producing the sg-Si TFTs, it is essential to control the position of Si grains and enlarge the Si grains. The μ-Czochralski (grain-filter) process allows us to control the positions of Si grains precisely and to enhance the grain growth with a long pulsed laser[2)]. However, it was very hard to develop the process on a large glass substrate, because the grain-filter, a small hole with a diameter of about 100 nm, has to be formed.

Technologies for fine patterning of large glass substrates have recently been developed; sub-micron poly-Si TFTs already existed[3)]. Using these technologies, we have successfully developed the μ-Czochralski process on a large glass substrate.

This paper describes the evaluation of Si grains prepared on a large glass substrate by the μ-Czochralski process with the fine patterning technologies. It also describes our investigation into characteristics of sg-Si TFTs and sub-micron sg-Si TFTs obtained from the process.

2. Experiments

The samples used in this study were fabricated through the μ-Czochralski process. Firstly, small holes with a diameter and a depth of 0.6 μm and 650 nm, respectively, are formed in a SiO_2 film on a 300 × 300 mm^2 glass substrate by using Holographic Mask Aligner (HMA) systems and Inductive Coupled Plasma (ICP) etching systems, by which sub-micron patterning on the substrate can be realized[3)]. Secondly, a 550-nm-thick TEOS PECVD SiO_2 film was deposited over the structure to reduce the hole diameter to around 100 nm. The resultant smaller holes are called a grain-filter. Thirdly, a-Si film with a thickness of 150 nm was deposited using LPCVD at 425°C on the SiO_2 film with the grain-filter. Lastly, the a-Si film was crystallized by a XeCl excimer laser with a duration time of about 200 ns at various energy densities. Some of the samples were heated at 400°C during the laser crystallization.

In the TFT fabrication process, oxygen plasma treatment was carried out after the laser crystallization. A gate insulator with a thickness of 40 nm was prepared by TEOS-PECVD, and annealed at 330°C for an hour in a steam ambient.

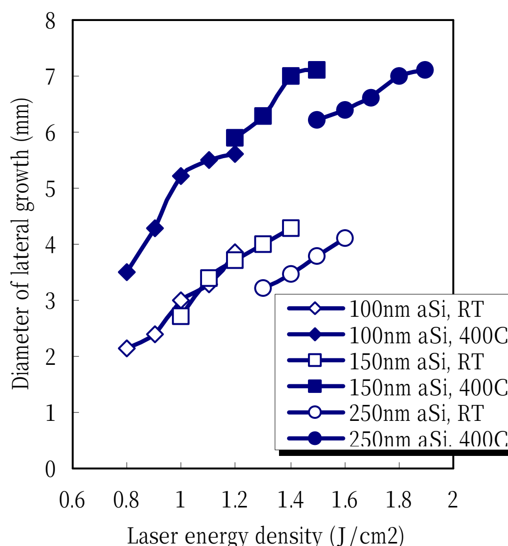

Fig. 1. Diameters of Si lateral growth as a function of laser energy density for various a-Si thickness and substrate temperatures.

3. Results and discussions

Figure 1 shows the diameters of Si grain growth after laser irradiation. The diameters increase with laser energy density and substrate temperature, and a maximum diameter of around 7 μm is obtained. This maximum diameter is larger than that prepared on a Si wafer as reported in AM-LCD'03[2]. An electron backscatter diffraction (EBSD) analysis showed that the Si grains included coincidence site lattice (CSL) boundaries like Σ3, Σ9 and Σ27 without random grain boundaries.

Figure 2(a) and 2(b) show cross-sectional TEM images of CSL boundaries located around the grain-filter. Crystal lattices with few defects and some planar faults can be observed in Fig. 2(b).

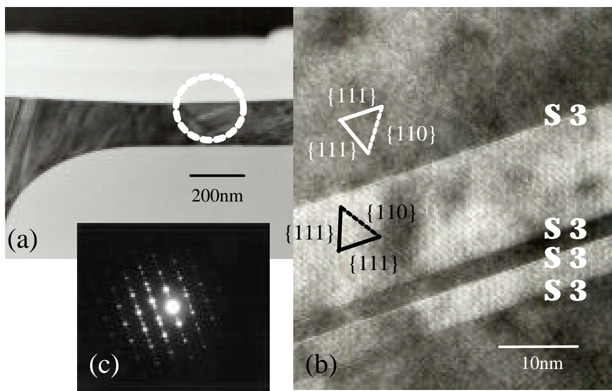

Fig. 2. Cross-sectional TEM images of CSL boundaries and an electron diffraction pattern of the observation area.

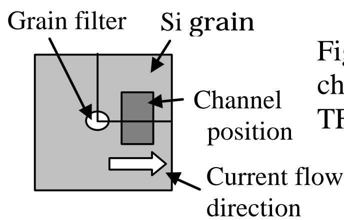

Fig. 3. Top view of channel position of TFT inside the grain

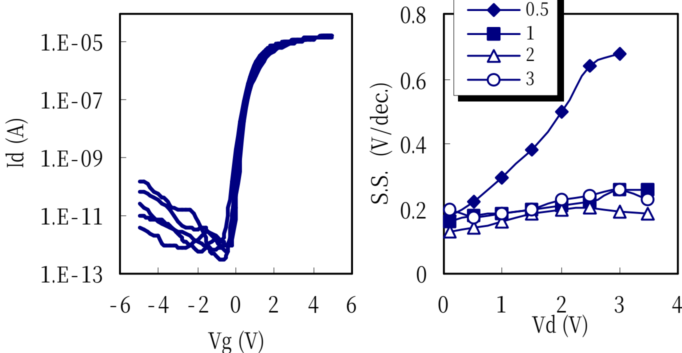

Fig. 4. Id-Vg characteristics of sg-Si TFTs.

Fig. 5. Subthreshold swings of sg-TFTs with various channel lengths.

According to identifications of the crystallographic orientations, the planar faults are parallel to {111} planes, and the misorientation between both sides is 70.5° rotation along the <110> axis, which corresponds to Σ3. These crystallographic orientations are also confirmed by an electron diffraction pattern as shown in Fig. 2(c).

In Raman spectroscopy analysis, a tensile stress of around 1×10^{10} dyn/cm^2, which is similar to that of conventional laser crystallized poly-Si film, was observed inside the Si grains.

Sg-TFTs with a Si film thickness of 150 nm were fabricated at a shifted position from the grain-filter as shown in Fig. 3 to avoid CSL boundaries around the grain-filter[2]. Figure 4 shows the transfer characteristics of the sg-Si TFTs with a channel length and a channel width of 1 μm and 1.7 μm, respectively. A field-effect mobility of 512 cm^2/Vs and a subthreshold swing of 0.16 V/dec. are obtained on average at a drain voltage (Vd) of 0.1 V. Figure 5 shows subthreshold swings of sg-TFTs with channel lengths of 0.5, 1, 2 and 3 μm as a function of Vd. The subthreshold swing of the sg-TFTs with a channel length of 0.5 μm increases with Vd. This is caused by a short channel effect with drain-induced barrier lowering (DIBL). This is also observed in output characteristics of the sub-micron sg-TFT as increments of source-drain leakage current. To avoid the DIBL, channel Si film thickness should be decreased.

4. Conclusions

Location-controlled large Si grains with few defects are prepared on a large glass substrate by the μ-Czochralski process. The sg-Si TFTs yielded by the process exhibited a high mobility of 512 cm^2/Vs and a low subthreshold swing of 0.16 V/dec. The sub-micron sg-Si TFT shows the short channel effect, which is due to relatively thick channel Si film.

References

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